Behavioral models of digital IC ports from measured transient waveforms

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Abstract: This paper addresses the behavioral modeling of output ports of digital integrated circuits via the identification of nonlinear parametric models. The aim of the approach is to produce models for SI simulation directly from the measured transient responses of devices. The modeling process is thoroughly described and an experimental demonstration of its feasibility is given.

1 Introduction

The numerical simulation of off-chip transmissions of fast digital signals requires effective models of the transmitting and receiving integrated circuits (ICs). Such models must be efficient and accurate enough to allow both the simulation of complex circuits and the prediction of critical Signal Integrity (SI) effects. Behavioral models meet such requirements and are establishing as the main resource for the description of IC ports.

A behavioral model of a device is a set of port characteristic equations obtained from external (possibly virtual) measurements. The most common approach to behavioral modeling is via simplified equivalent circuits of IC ports, because equivalents allow physical insight and facilitate the implementation of models. An important example of the equivalent circuit approach to behavioral modeling is the widely adopted Input/output Buffer Information Specification (IBIS). IBIS offers high numerical efficiency, large data library and commercial software tools handling models and complex modeling problems. The equivalent circuit approach to behavioral modeling, however, has also inherent limitations. Mainly the identification of model parameters is easy only by virtual measurements, *i.e.*, from transistor-level models of the devices, and the physical effects taken into account by the model are decided a priori, when the equivalent circuit defining the model is selected. In order avoid such limitations, in this work we explore the modeling of digital IC ports via the identification of nonlinear dynamic parametric models. Such an approach amounts to seek approximate port characteristic equations of devices and has interesting advantages. Parametric models can be effectively generated from actual measurements, as their identification requires only input and output waveforms. They automatically take into account all the physical effects relating input and output data, for their structure is selected by the identification process itself. As an example, when package parasitics and the nonlinear dynamics of the output transistors contribute to the evolution of the output waveforms, they are automatically included in the model. Finally, parametric models have inherent low sensitivity to the load they drive, which means loads used to measure the output waveforms are not relevant and the obtained models can drive many different loads.

2 Parametric models of IC output ports

In order to discuss the proposed modeling approach, we focus on the modeling of an output port of a digital IC. In this case, the Device Under Modeling (DUM) is an output buffer of an IC. Such a DUM is a 2-port element, whose output port is the observed output port of the IC, and whose input port is on the chip. The parametric model, therefore, must relate voltage and current of the selected output pin (v and i, respectively, with outcoming current reference direction) and the voltage of the buffer input port, that cannot be measured. For this modeling problem, we develop the following 2-piece parametric model [1], that can be identified simply from the v and i waveforms

$$\begin{aligned} i(k) &= w_1(k) f_1(\Theta_1, \mathbf{x}(k)) + w_2(k) f_2(\Theta_2, \mathbf{x}(k)) \\ f_n(\Theta_n, \mathbf{x}(k)) &= \sum_j \theta_{nj} \exp\{-|\mathbf{x} - \mathbf{c}_{nj}|^2/\beta^2\}, \qquad n = 1, 2 \\ \mathbf{x}^T(k) &= [i(k-1), \ldots, i(k-r), v(k), v(k-1), \ldots, v(k-r)] \end{aligned} \tag{1}$$

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In the above equation, i is the output variable of the model, f_1 and f_2 are two radial basis function submodels predicting i for varying v and constant logic state, whereas vectors $w_1(k)$ and $w_2(k)$ are time varying weight coefficients that take into account the evolution of the port logic state and act as switches between submodels f_1 and f_2, and, finally, vectors Θ_n collect the unknown parameters $\{\theta_{nj}, \mathbf{c}_{nj}, \beta\}$ that must be determined from a suitable set of measured waveforms [2]. Each weight coefficient w_n is obtained by means of a concatenation of two basic sequences $w_n^u(k)$ and $w_n^d(k)$, that describe the "up" and the "down" logic state transitions of the port, respectively. The sequences of the two transitions occur in alternate order and are issued synchronously with the changes of the logic inputs controlling the state of the DUM. Of course, such a simplified model holds only for logic state transitions spaced enough in time, so that every new transition starts after the previous one has been completed. However, since the above validity condition is satisfied in properly working digital circuits, it does not limit the use of the model in SI simulation problems. Indeed the parametric model (1) allows to exploit the advantages outlined in Sec. 1. It is easy to identify and, even with a few basis functions (*e.g.*, $p \in [5, 20]$), the identified models track accurately the behavior of most output buffer circuits for a large set of possible driven loads.

3 Modeling process

The modeling of an IC port via the proposed approach can be divided into three parts: (I) the excitation and recording of transient responses of the DUM, (II) the identification of the model parameters Θ_n and w_n, $n = 1, 2$, from the recorded transient responses, and (III) the implementation of the obtained model in a standard circuit simulation environment (*e.g.*, Spice).

Part (I) amounts to drive the DUM to obtain transient output signals carrying information on its behavior. The excitation and response signals involved in this step are named ***identification signals.*** In our problem, we need two sets of identification signals: the steady state identification signals, for submodels f_1 and f_2, and the switching identification signals, for the weight coefficients w_1 and w_2.

Submodels f_1 and f_2 yield the current response $i(t)$ caused by $v(t)$ at fixed logic state. The steady state identification signals, therefore, are composed of a driving voltage waveform applied to the port (submodel input variable) and of its corresponding current response (submodel output variable). The driving waveform must be carefully designed, in order to excite every possible dynamic behavior of the system under modeling. Such a design, however, is a critical point of every nonlinear identification problem, because only qualitative guidelines are available [3]. Typical driving waveforms are multilevel signals spanning the whole range of allowed input values with suitable duration and added noise. The selection of the driving waveform is a matter of repeated identification experiments, where the ability of different identification signals to yield good quality models is verified over a set of sample systems. In order to obtain driving waveform that can be synthesized by standard waveform generators, we look for the simplest driving waveform ensuring successful identification. Our optimum choice are voltage waveforms composed of three to four level transitions over the range $[V_{ss} - \Delta, V_{cc} + \Delta]$, where Δ is the accepted overvoltage, and edges with rise/fall times comparable to the switching times of the port. The flat parts of the waveform last enough to allow the DUM to reach steady state operation and no noise signal are added (*e.g.*, see Fig. 3).

Once f_1 and f_2 are identified, the weight coefficients w_1 and w_2 are obtained from a set of switching identification signals by linear inversion of (1), *i.e.*,

$$\begin{bmatrix} w_1(k) \\ w_2(k) \end{bmatrix} = \begin{bmatrix} f_1(\Theta_1, \mathbf{x}_a) & f_2(\Theta_2, \mathbf{x}_a) \\ f_1(\Theta_1, \mathbf{x}_b) & f_2(\Theta_2, \mathbf{x}_b) \end{bmatrix}^{-1} \begin{bmatrix} i_a(k) \\ i_b(k) \end{bmatrix} \tag{2}$$

In the above equation, waveforms $\{i_a, v_a\}$ and $\{i_b, v_b\}$ are the switching identification signals, which are recorded when the output port drives two different loads (load (a) and load (b)) and complete state switchings are caused by variations of the logic inputs. To be more precise, the basic sequences (see Sec. 2) w_1^u and w_2^u (w_1^d and w_2^d) are computed from $\{i_a^u, v_a^u\}$ and $\{i_b^u, v_b^u\}$ ($\{i_a^d, v_a^d\}$ and $\{i_b^d, v_b^d\}$) recorded during a LOW to HIGH (HIGH to LOW) transition. There are no restrictions on load (a) and load (b), which can be also real sources stimulating the output port. The best loads would be those allowing $\{i_a, v_a\}$ and $\{i_b, v_b\}$ to explore the widest possible region of the v-i plane. We do not yet address the optimization of such loads. Presently we use the same loads recommended by IBIS to characterize port switchings, *i.e.*, load (a) is a resistor and load (b) is a series connection of a resistor and a battery.

In part (II) we compute the model parameters from the identification signal obtained in part (I) of the modeling process. As described above, the evaluation of the weight coefficients $w_n(k)$ is a straightforward operation, that follows the identification of submodels f_n and is carried out via the closed form equation (2). Submodels f_1 and f_2, instead, must be obtained from the steady state identification signals via an

actual identification algorithm. We use the algorithm of [4] that works by minimizing the mean square error between the identification output signals and the model output. Such an algorithm enables a Penthium PC to identify submodels with $10 \div 20$ radial basis functions in a few seconds.

Finally, in part (III) of the modeling process, the identified input-output discrete-time model is replaced by a continuous-time state-space model, in order to be easily coded as a macromodel of circuit simulators like Spice. Such a conversion is achieved by replacing back the time variable in (1) ($t = kT$, where T is the sampling time used to sample the input and output waveforms) and by approximating the difference operator with the differential one (*e.g.*, $\dot{z}(t) \simeq \frac{1}{T}[z(kT) - z(kT - T)]$). The implementation of the continuous-time model is obtained by the equivalent circuits of its state-space equations, that are RC circuits with controlled sources.

4 Experimental results

The proposed approach has been tuned by the identification of several virtual devices, that are transistor-level models of typical output buffers. In order to verify its practical feasibility, *i.e.*, that measurement errors and noise do not prevent its application, we verify it on a real device: a NAND gate of an HC7400 IC connected as inverter. Such a DUM is both sufficiently simple and representative to be an easy and significant test case.

For a real device, a text fixture suitable to apply and measure signals is needed. The main point is that, in a real setup, ideal voltage sources are not available and, therefore, the identification voltage waveform cannot be directly imposed. The remedy is to stimulate the DUM by a common waveform generator and to measure both i and v of the output port. The parameter of the waveform generator are then tuned till the observed voltage waveform has the requested behavior (see Sec. 3). The measurement of the output current i can be performed by either a wideband current probe or, indirectly, by a series resistor. We choose the series resistor arrangement and assembled the test fixture shown in Fig. 1.

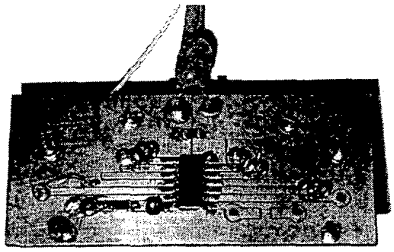

Figure 1: Test fixture.

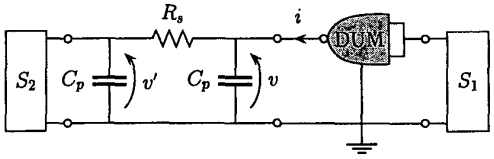

Figure 2: Equivalent circuit of the identification setup ($R_s = 100\,\Omega, C_p = 14.1\,\text{pF}$). S_1 and S_2 are the sources of the identification signals.

An SMD $100\,\Omega$ resistor is connected in series to the output pin of one of the four NAND gates of the HC7400, whereas SMA connectors are placed on the back of the board to inject and probe signals. The voltages at the terminals of the series resistor are simultaneously recorded by an oscilloscope Tektronix TDS380 (sampling pitch $T = 200\,\text{ps}$) and passive voltage probes P6114B. The current waveform is extracted from the two recorded voltage waveforms via the equivalent circuit shown in Fig. 2 as $i = C_p dv/dt + (v - v')/R_s$. In such a circuit the shunt capacitors at the terminals of the series resistor represent the parasitics of probes.

The steady state identification signals are generated by using a Rhode&Schwarz AFS multifunction waveform synthesizer connected as S_2 while the DUM input is set, via source S_1, to either the HIGH or the LOW logic output state. The steady state identification signals obtained in this way for the submodel f_1 are shown in Fig. 3. The waveform generator to excite such signals is not a critical element. In this setup, the shaping of the identification signal is obtained by a stub element connected between S_2 and the test fixture. In a setup for routine measurements, the waveform generator could be provided by a dedicated circuit composed of discrete logic gates. The switching identification signal, finally, are obtained by replacing S_2 with a $50\,\Omega$ coax resistor and with a $60\,\Omega$ carbon resistor connected to V_{cc} as load (a) and load (b), respectively, and by driving (via S_1) the DUM to produce a HIGH pulse.

The identified model turns out to be composed of two submodels with dynamic order $r = 1$ and number

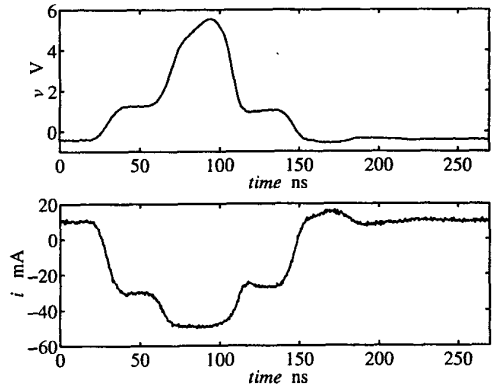

Figure 3: Measured steady state identification signals $v(t)$ and $i(t)$ for submodel f_1.

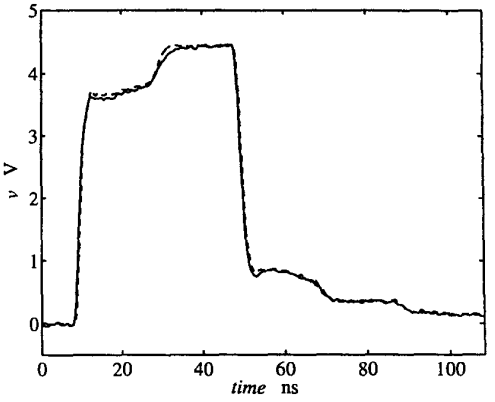

Figure 4: Output voltage waveform of the DUM driving a series connection of a 100 Ω resistor and an open ended 1.5 m long RG58 coaxial cable ($Z_0 = 50\,\Omega$). Dashed line: measured reference response; solid line: response of the 2-piece RBF model.

of basis functions $p = 5$. Figure 4 shows the result of a validation test for such a model, the two curves are the measured response of the DUM and the computed response of the identified model when they send a pulse on the series connection of R_s and an open ended RG58 coaxial cable (see Fig. 2). Such a comparison shows that the identified model performs at a very good accuracy level. Besides, it is ought to remark that, in this example, modeling and validation are based on a rather idealized equivalent circuit of the test fixture.

5 Conclusion

This paper addresses the behavioral modeling of digital IC ports via the identification of nonlinear parametric models. The aim of the proposed approach is to enable any user to easily model poorly documented devices just from measured transient responses and to use the obtained models to assess SI effects on critical nets by standard circuit simulators.

The loads involved in the measurement of the transient responses are not relevant to the identified models, which work accurately for different loads. Also, all the elements that may contribute to the responses of the IC port, as package parasitics and the nonlinear dynamics of the output transistors, are automatically included. Owing to such features, the parametric approach could be easily extended to include other effects, like the simultaneous switching of ports, or to model other ports like, the V_{cc}, V_{ss} port.

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